Notice of Allowability	Application No.	Applicant(s)	
	10/688,550	KIM ET AL.	
	Examiner	Art Unit	
	John H. Le	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to _____.

2. ☒ The allowed claim(s) is/are *1-12*.

3. ☒ The drawings filed on *10 February 2004* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 10/17/2003
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Reasons for Allowance

1. Claims 1-12 are allowed.

2. The following is an examiner's statement of reasons for allowance:

Regarding claim 1, none of the prior art of record teaches or suggests the combination of a method for quantifying a plurality of safe operating regions within a safe operating area (SOA) for a bipolar junction transistor (BJT), wherein the method comprising steps of: providing a current mirror circuit with mutually coupled first and second BJTS, wherein said first BJT includes a base electrode, a collector electrode and an emitter electrode with an area, said second BJT includes a base electrode, a collector electrode and an emitter electrode with an area, and said second BJT emitter area is greater than said first BJT emitter area; applying an inter-electrode voltage with a plurality of values to first and second ones of said second BJT electrodes; applying a first current with a plurality of values to at least one of said first BJT electrodes; measuring a plurality of values of a second current through one of said second BJT electrodes corresponding to a plurality of combinations of said pluralities of inter-electrode voltage and first current values; computing a plurality of electrode current densities corresponding to a plurality of ratios of said plurality of second current values and said second BJT emitter electrode area; computing a plurality of ratios of said second and first current values corresponding to at least a portion of said plurality of combinations of said pluralities of inter-electrode voltage and first current values; computing a plurality of ratio errors corresponding to a plurality of differences between each one of said plurality of second and first

current ratios and a reference current ratio. It is these limitations as they are claimed in the combination with other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Regarding claim 7, none of the prior art of record teaches or suggests the combination of a method for quantifying a plurality of safe operating regions within a safe operating area (SOA) for a bipolar junction transistor (BJT), wherein the method comprising steps of: providing a plurality of transistor model data for first and second BJTS, wherein said first BJT includes a base electrode, a collector electrode and an emitter electrode with an area, said second BJT includes a base electrode, a collector electrode and an emitter electrode with an area, and said second BJT emitter area is greater than said first BJT emitter area; simulating a current mirror circuit with said plurality of transistor model data, wherein said first and second BJTS are mutually coupled; simulating an application of an inter-electrode voltage with a plurality of values to first and second ones of said second BJT electrodes; simulating an application of a first current with a plurality of values to at least one of said first BJT electrodes; computing a plurality of values of a second current through one of said second BJT electrodes corresponding to a plurality of combinations of said pluralities of inter-electrode voltage and first current values; computing a plurality of electrode current densities corresponding to a plurality of ratios of said plurality of second current values and said second BJT emitter electrode area; computing a plurality of ratios of said second and first current values corresponding to at least a

portion of said plurality of combinations of said pluralities of inter-electrode voltage and first current values; computing a plurality of ratio errors corresponding to a plurality of differences between each one of said plurality of second and first current ratios and a reference current ratio. It is these limitations as they are claimed in the combination with other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

U.S. Patent No. 6,121,089 discloses techniques to improve the safe operating area (SOA) of power devices by making them less susceptible to destructive voltage breakdown have also included the use of clamping regions which extends between adjacent unit cells of a power MOSFET or between adjacent unit cells of an insulated-gate bipolar junction transistor (IGBT). Methods of forming power semiconductor devices having merged split-well body regions include the steps of forming a semiconductor substrate containing a drift region of first conductivity type (e.g., N-type) therein extending to a first face thereof. '089 fails to specify the steps of providing a current mirror circuit with mutually coupled first and second BJTS, wherein said first BJT includes a base electrode, a collector electrode and an emitter electrode with an area, said second BJT includes a base electrode, a collector electrode and an emitter electrode with an area, and said second BJT emitter area is greater than said first BJT emitter area; applying an inter-electrode voltage with a plurality of values to first and second ones of said second BJT electrodes; applying a first current with a plurality of values to at least one of said first BJT electrodes;

measuring a plurality of values of a second current through one of said second BJT electrodes corresponding to a plurality of combinations of said pluralities of inter-electrode voltage and first current values; computing a plurality of electrode current densities corresponding to a plurality of ratios of said plurality of second current values and said second BJT emitter electrode area, as now recited in claim 1 of the present invention. '089 also fails to specify the steps of providing a plurality of transistor model data for first and second BJTS, wherein said first BJT includes a base electrode, a collector electrode and an emitter electrode with an area, said second BJT includes a base electrode, a collector electrode and an emitter electrode with an area, and said second BJT emitter area is greater than said first BJT emitter area; simulating a current mirror circuit with said plurality of transistor model data, wherein said first and second BJTS are mutually coupled; simulating an application of an inter-electrode voltage with a plurality of values to first and second ones of said second BJT electrodes; simulating an application of a first current with a plurality of values to at least one of said first BJT electrodes; computing a plurality of values of a second current through one of said second BJT electrodes corresponding to a plurality of combinations of said pluralities of inter-electrode voltage and first current values, as now recited in claim 7 of the present invention.

U.S. Patent No. 5,909,039 discloses an insulated gate bipolar transistor (IGBT) of the type defined in the introduction, which is simply constructed and has a large safe operating area due to a high latch up tolerance, obtained by arranging a layer having a contact portion vertically separated from the source

region layer and having the source applied thereon for collecting holes injected from the substrate layer to the drift layer at a vertical distance from the source region layer. '039 fails to specify the steps of providing a current mirror circuit with mutually coupled first and second BJTS, wherein said first BJT includes a base electrode, a collector electrode and an emitter electrode with an area, said second BJT includes a base electrode, a collector electrode and an emitter electrode with an area, and said second BJT emitter area is greater than said first BJT emitter area; applying an inter-electrode voltage with a plurality of values to first and second ones of said second BJT electrodes; applying a first current with a plurality of values to at least one of said first BJT electrodes; measuring a plurality of values of a second current through one of said second BJT electrodes corresponding to a plurality of combinations of said pluralities of inter-electrode voltage and first current values; computing a plurality of electrode current densities corresponding to a plurality of ratios of said plurality of second current values and said second BJT emitter electrode area, as now recited in claim 1 of the present invention. '0389 also fails to specify the steps of providing a plurality of transistor model data for first and second BJTS, wherein said first BJT includes a base electrode, a collector electrode and an emitter electrode with an area, said second BJT includes a base electrode, a collector electrode and an emitter electrode with an area, and said second BJT emitter area is greater than said first BJT emitter area; simulating a current mirror circuit with said plurality of transistor model data, wherein said first and second BJTS are mutually coupled; simulating an application of an inter-electrode voltage with a

plurality of values to first and second ones of said second BJT electrodes; simulating an application of a first current with a plurality of values to at least one of said first BJT electrodes; computing a plurality of values of a second current through one of said second BJT electrodes corresponding to a plurality of combinations of said pluralities of inter-electrode voltage and first current values, as now recited in claim 7 of the present invention.

U.S. Patent No. 5,557,139 discloses a vertical bipolar power transistor with a buried base and interdigitated construction, having a similarly buried emitter region, and at least one elongate portion connected to a surface emitter electrode through an interconnection region of predetermined resistively, which transistor has none of the drawbacks besetting the prior art transistor, namely exhibits a higher current gain and a larger safe operation area, with all the other conditions being equal. '139 fails to specify the steps of providing a current mirror circuit with mutually coupled first and second BJTS, wherein said first BJT includes a base electrode, a collector electrode and an emitter electrode with an area, said second BJT includes a base electrode, a collector electrode and an emitter electrode with an area, and said second BJT emitter area is greater than said first BJT emitter area; applying an inter-electrode voltage with a plurality of values to first and second ones of said second BJT electrodes; applying a first current with a plurality of values to at least one of said first BJT electrodes; measuring a plurality of values of a second current through one of said second BJT electrodes corresponding to a plurality of combinations of said pluralities of inter-electrode voltage and first current values; computing a plurality of electrode

current densities corresponding to a plurality of ratios of said plurality of second current values and said second BJT emitter electrode area, as now recited in claim 1 of the present invention. '139 also fails to specify the steps of providing a plurality of transistor model data for first and second BJTS, wherein said first BJT includes a base electrode, a collector electrode and an emitter electrode with an area, said second BJT includes a base electrode, a collector electrode and an emitter electrode with an area, and said second BJT emitter area is greater than said first BJT emitter area; simulating a current mirror circuit with said plurality of transistor model data, wherein said first and second BJTS are mutually coupled; simulating an application of an inter-electrode voltage with a plurality of values to first and second ones of said second BJT electrodes; simulating an application of a first current with a plurality of values to at least one of said first BJT electrodes; computing a plurality of values of a second current through one of said second BJT electrodes corresponding to a plurality of combinations of said pluralities of inter-electrode voltage and first current values, as now recited in claim 7 of the present invention.

U.S. Patent No. 4,941,030 discloses a bipolar transistor having a collector layer on a semiconductor substrate, a base layer formed on the collector layer and an emitter island formed in the base layer region, at least one groove is formed to reach at least the interface between the base layer and the collector layer from the surface of the bipolar transistor in the interior or peripheral region of the emitter island, so as to be employed as a gate electrode of a MOS-FET. The bipolar transistor performs operation in a quasi-saturated or active region by

the constant-voltage diode provided between the gate and the base, whereby stored charges are reduced and the reverse bias base current of the bipolar transistor is extremely reduced, which results that a reverse bias safe operating area is increased. '030 fails to specify the steps of providing a current mirror circuit with mutually coupled first and second BJTS, wherein said first BJT includes a base electrode, a collector electrode and an emitter electrode with an area, said second BJT includes a base electrode, a collector electrode and an emitter electrode with an area, and said second BJT emitter area is greater than said first BJT emitter area; applying an inter-electrode voltage with a plurality of values to first and second ones of said second BJT electrodes; applying a first current with a plurality of values to at least one of said first BJT electrodes; measuring a plurality of values of a second current through one of said second BJT electrodes corresponding to a plurality of combinations of said pluralities of inter-electrode voltage and first current values; computing a plurality of electrode current densities corresponding to a plurality of ratios of said plurality of second current values and said second BJT emitter electrode area, as now recited in claim 1 of the present invention. '030 also fails to specify the steps of providing a plurality of transistor model data for first and second BJTS, wherein said first BJT includes a base electrode, a collector electrode and an emitter electrode with an area, said second BJT includes a base electrode, a collector electrode and an emitter electrode with an area, and said second BJT emitter area is greater than said first BJT emitter area; simulating a current mirror circuit with said plurality of transistor model data, wherein said first and second BJTS are mutually coupled;

simulating an application of an inter-electrode voltage with a plurality of values to first and second ones of said second BJT electrodes; simulating an application of a first current with a plurality of values to at least one of said first BJT electrodes; computing a plurality of values of a second current through one of said second BJT electrodes corresponding to a plurality of combinations of said pluralities of inter-electrode voltage and first current values, as now recited in claim 7 of the present invention.

U.S. Patent No. 4,823,176 discloses an increase in the safe operating area of a semiconductor field effect device by modifying the shape of its base region so that the high voltage blocking PN junction formed between the base region and the more lightly doped body region intersects the semiconductor surface and encloses an area of the body region at that surface which is a closed plane geometrical figure which is everywhere convex or whose maximum width is less than about the depletion width of the high voltage junction in the body region at breakdown. To maximize the breakdown voltage, the maximum radius of curvature of the boundary of the geometric figure is made small and is preferably substantially less than the depletion width of a corresponding parallel plane PN junction at its breakdown voltage. '176 fails to specify the steps of providing a current mirror circuit with mutually coupled first and second BJTS, wherein said first BJT includes a base electrode, a collector electrode and an emitter electrode with an area, said second BJT includes a base electrode, a collector electrode and an emitter electrode with an area, and said second BJT emitter area is greater than said first BJT emitter area; applying an inter-electrode voltage with a

plurality of values to first and second ones of said second BJT electrodes; applying a first current with a plurality of values to at least one of said first BJT electrodes; measuring a plurality of values of a second current through one of said second BJT electrodes corresponding to a plurality of combinations of said pluralities of inter-electrode voltage and first current values; computing a plurality of electrode current densities corresponding to a plurality of ratios of said plurality of second current values and said second BJT emitter electrode area, as now recited in claim 1 of the present invention. '176 also fails to specify the steps of providing a plurality of transistor model data for first and second BJTS, wherein said first BJT includes a base electrode, a collector electrode and an emitter electrode with an area, said second BJT includes a base electrode, a collector electrode and an emitter electrode with an area, and said second BJT emitter area is greater than said first BJT emitter area; simulating a current mirror circuit with said plurality of transistor model data, wherein said first and second BJTS are mutually coupled; simulating an application of an inter-electrode voltage with a plurality of values to first and second ones of said second BJT electrodes; simulating an application of a first current with a plurality of values to at least one of said first BJT electrodes; computing a plurality of values of a second current through one of said second BJT electrodes corresponding to a plurality of combinations of said pluralities of inter-electrode voltage and first current values, as now recited in claim 7 of the present invention.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should

preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Contact Information

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John H Le whose telephone number is 571-272-2275. The examiner can normally be reached on 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E Barlow can be reached on 571-272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John H. Le

Patent Examiner-Group 2863

March 31, 2005

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